CBCS SCHEME

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18EC644

Sixth Semester B.E. Degree Examination, July/August 2022
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Develop a verilog model for a 4:1 multiplexer. **(04 Marks)**

b. Explain with illustration, a simple design methodology followed in IC industries. **(08 Marks)**

c. Develop verilog model for a 7-segment decoder, include an additional input, blank that overrides the BCD input and causes all segments not to be lit. **(08 Marks)**

OR

2 a. With a neat block diagram, explain a design methodology for hardware/software co-design. **(10 Marks)**

b. Develop a verilog model of the priority encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Sensor signal is '1' when an instrusion is detected in that zone and '0' otherwise. Zone 1 is having highest priority, down to zone 8 having lowest priority. **(10 Marks)**

Module-2

3 a. Determine whether there is an error in the ECC word 000111000100 and if so correct it. **(06 Marks)**

b. Design a 64K × 8 bit composite memory using four 16K × 8 bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. **(08 Marks)**

c. Explain about the multiport memories. **(06 Marks)**

OR

4 a. What is the difference between asynchronous static RAM and synchronous static RAM? **(08 Marks)**

b. Develop a verilog model of a dual port 4K × 16 bit flow through SSRAM. One port allows data to be written and read, while the other port allows data to be read. **(08 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word '01100001'. **(04 Marks)**

Module-3

5 a. Outline and explain the internal organization of FPGA. **(10 Marks)**

b. Briefly explain programmable array logic. **(10 Marks)**

OR

6 a. Explain the concept differential signaling. How does differential signaling improve noise immunity? **(10 Marks)**

b. What distinguishes a platform FPGA from a simple FPGA? **(05 Marks)**

c. Explain different types of PCB design. **(05 Marks)**

Module-4

7 a. With a neat diagram, explain R-string DAC and R/2R ladder DAC. **(10 Marks)**

b. Explain any four serial interface standards. **(10 Marks)**

OR

8 a. Explain any four analog sensors. **(10 Marks)**

b. Explain flash ADC and successive approximation ADC with the help of necessary diagrams. **(10 Marks)**

Module-5

9 a. Explain briefly area, power and timing optimization in digital circuits. **(10 Marks)**

b. Explain fault model and fault simulation. **(10 Marks)**

OR

10 a. Demonstrate Built-In Self Test (BIST) techniques. **(10 Marks)**

b. Explain the hardware and software co-design flow. **(10 Marks)**

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